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10/607,983	06/30/2003	Jong Jin Park	8733.890.00	6985

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EXAMINER	
SHERMAN, STEPHEN G	

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 09/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/607,983	PARK ET AL.	
	Examiner	Art Unit	
	Stephen G. Sherman	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because of undue length. The abstract is more than 150 words. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 18 and claim 9, both dependent on claim 1, claim the same limitation. Therefore claim 18 is rejected since the limitation was already brought forth in claim 9. See 37 C.F.R. § 1.75 (b). For examination purpose, claim 18 will be considered dependent on claim 10.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over APA, in view of Kwag (US 2002/0015017).

Regarding claim 1, APA discloses a liquid crystal display having a normal drive period when liquid crystals are normally driven after alignment of the liquid crystals injected between upper/lower plates (Paragraph [0017] states: "a liquid crystal 18 injected into a designated gap between the upper substrate 10 and the lower substrate 12") is changed from a splay state to a bend state at a voltage higher than a transition voltage (Paragraph [0018] states: "The liquid crystal molecules having such a splay state are changed into a bend state at a voltage more than the specified voltage Vtr."), comprising: a liquid crystal display panel having a thin film transistor at each intersection part of a plurality of data lines and a plurality of gate lines (Paragraph [0005]); a gate driver (Figure 1, item 4) configured to supply a gate high voltage and a gate low voltage during a data input period (Figure 4, Vgh and Vgl); a data driver (Figure 1, item 6) configured to supply data voltages to the data lines in accordance with gate voltages

applied to the gate lines (Paragraph [0010] states: "The TFT supplies data voltages Vd from the data lines DL1 to DLm to the liquid crystal cell Clc in response to the gate high voltage Vgh from the gate lines GL1 to GLn."); and a timing controller configured to control the data voltages supplied to the data lines and the gate voltages supplied to the gate lines (Figure 1, item 8 and paragraph [0006]). APA fails to teach of a liquid crystal device comprising a gate driver configured to sequentially supply a gate reset voltage to gate lines during a reset period, wherein the normal drive period is divided into the data input period and the reset period. Kwag discloses a liquid crystal device comprising a gate driver (Figure 2, item 20) configured to sequentially supply a gate reset voltage to gate lines during a reset period (Figure 7A), wherein the normal drive period is divided into the data input period and the reset period (Figure 5, items T1, T2 and T3. Paragraph [0065] states: "...T1 is a reset interval, T2 is a gate-on interval, and T3 is an overshoot interval" The examiner interprets the normal drive period to consist of T1, T2 and T3 where T1 is the reset period and T2 and T3 combine to form the data input period.). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teaching of APA and Kwag in order to provide a liquid crystal display that can reset its gate lines before each transmission of data.

Regarding claim 2, APA and Kwag disclose the liquid crystal display according to claim 1. APA also discloses wherein the gate driver is configured to supply the gate high voltage to the gate lines during an on-period for the thin film transistor in the data input period (Paragraph [0012] where it states: "Scan pulses (SP) with the gate high voltage Vgh turn on the TFT switch..."), and to supply the gate low voltage to the gate

lines during an off-period for the thin film transistor (Paragraph [0012] where it states: "As the gate high voltage Vgh supplied to the gate lines GL1 to GLn is changed to the gate low voltage Vgl, the TFT is turned off..."). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teaching of APA and Kwag in order to only have the TFT on when data signals are being sent.

Regarding claim 3, APA and Kwag disclose the liquid crystal display according to claim 1. Kwag also discloses wherein the gate reset voltage is a designated voltage set to be lower than the gate low voltage (In Figure 7B, Vg(n-1), the voltage during the reset period is less than the voltage line during the overshoot interval, where the overshoot interval is when the gate low voltage is applied). Therefore it would have obvious to "one of ordinary skill" in the art to combine the teachings of APA and Kwag in order to reduce the average voltage of the liquid crystal display.

6. Claims 4, 6 and 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over APA and Kwag (US 2002/0015017) and further in view of Ono et al. (US 6,057,817).

Regarding claim 4, APA and Kwag disclose the liquid crystal display according to claim 1. APA and Kwag fail to teach of a liquid crystal device wherein the gate reset voltage and the gate low voltage, which are alternately applied to a previous gate line, constitute an AC voltage. Ono et al. disclose a liquid crystal device wherein the gate reset voltage and the gate low voltage, which are alternately applied to a previous gate line, constitute an AC voltage (Figure 32, where T_{S1} is the reset period in which $-V_R$ is

the reset voltage and $+V_R$ is the gate low voltage, which are alternated applied during T_{S1}.). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings APA, Kwag and Ono et al. in order to produce a liquid crystal display which has a reset period consisting of an AC voltage which allows for a decrease in power consumption by the liquid crystal while still providing for the average voltage applied to the liquid crystal to be higher than a transition voltage to prevent the display from changing into a splay state.

Regarding claim 6, APA, Kwag and Ono et al. disclose the liquid crystal display according to claim 4. Ono et al. also disclose wherein the gate low voltage applied for the data input period is the same as an average value of the AC voltage (Figure 32, The data input period is T_D, where in the gate low voltage shown in the figure is the same as the average value of $-V_R$ and $+V_R$, which combine to form the AC voltage). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings of APA, Kwag and Ono et al. in order to create a liquid crystal display that when the gate low voltage is applied during the data input period the average voltage applied to the liquid crystal is still higher than a transition voltage to prevent the display from changing into a splay state.

Regarding claim 8, APA and Kwag disclose the liquid crystal display according to claim 1. APA and Kwag fail to teach of a liquid crystal display device wherein the gate reset voltage is an AC voltage having positive and negative polarities alternated on the basis of the gate low voltage for each frame. Ono et al. also discloses wherein the gate reset voltage is an AC voltage having positive and negative polarities alternated on the

basis of the gate low voltage for each frame (Figure 32, T_{S1} is the reset period and $+V_R$ is the positive polarity and $-V_R$ is the negative polarity. $+V_R$ and $-V_R$ are alternated based on the gate low voltage, which is 0 during the period T_S). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings APA, Kwag and Ono et al. in order to produce a liquid crystal display which alternates between positive and negative polarities which allows for a decrease in power consumption by the liquid crystal while still providing for the average voltage applied to the liquid crystal to be higher than a transition voltage to prevent the display from changing into a splay state.

Regarding claim 9, APA and Kwag disclose the liquid crystal display according to claim 1. APA and Kwag fail to teach of a liquid crystal device wherein the gate reset voltage is an AC voltage. Ono et al. disclose a liquid crystal device wherein the gate reset voltage is an AC voltage (Figure 32, $+V_R$ and $-V_R$ constitute as an AC voltage). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings APA, Kwag and Ono et al. in order to produce a liquid crystal display which has an AC reset voltage which allows for a decrease in power consumption by the liquid crystal while still providing for the average voltage applied to the liquid crystal to be higher than a transition voltage to prevent the display from changing into a splay state.

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over APA and Kwag (US 2002/0015017) and further in view of Kondoh (US 6,509,887). APA and Kwag disclose the liquid crystal display according to claim 1. APA and Kwag fail to

teach of a liquid crystal display wherein the gate high voltage is applied at least two times for the data input period. Kondoh discloses a liquid crystal display wherein the gate high voltage is applied at least two times for the data input period (Figure 9 shows TS as the drive period, which consists of a reset period RS and a data input period made up of Se and NSe. The gate high voltage is applied during the two Se periods where in the second period the polarity is inverted, which the examiner interprets to mean that the gate high voltage is applied twice during the data input period.). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings of APA, Kwag and Kondoh et al. in order to compensate for the DC component which is created to cause the pixel voltage applied to the liquid crystal cell on the liquid crystal display panel to be biased to the negative polarity.

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over APA, Kwag (US 2002/0015017) and Ono et al. (US 6,057,817) and further in view of Kondoh (EP 1,043,618 A1). APA, Kwag and Ono et al. disclose the liquid crystal display according to claim 4. APA, Kwag and Ono et al. fail to disclose wherein a half period of the AC voltage is set to be less than a response time of the liquid crystals. Kondoh discloses a liquid crystal display wherein a half period of the AC voltage is set to be less than a response time of the liquid crystals (Column 9, lines 48-50. The examiner interprets that since the bipolar pulse, AC voltage, duration is 100μs that the half period is 50μs, which is much less than the response time of the liquid crystals since it is well known that liquid crystal response times are longer than 50μs). Therefore it would have

been obvious to "one of ordinary skill" in the art to combine the teachings of APA, Kwag, Ono et al. and Kondoh in order to prevent to the liquid crystals from responding and thus improving the brightness of the display.

9. Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over APA in view of Kondoh (EP 1,043,618 A1).

Regarding claim 10, APA discloses a driving method of a liquid crystal display having a normal drive period when liquid crystals are normally driven after alignment of, the liquid crystals injected between upper/lower plates (Paragraph [0017] states: "a liquid crystal 18 injected into a designated gap between the upper substrate 10 and the lower substrate 12") is changed from a splay state to a bend state at a voltage higher than a transition voltage (Paragraph [0018] states: "The liquid crystal molecules having such a splay state are changed into a bend state at a voltage more than the specified voltage Vtr."), comprising: forming a thin film transistor at each intersection part of a plurality of data lines and a plurality of gate lines (Paragraph [0005]); supplying a gate high voltage and a gate low voltage to the gate lines for the data input period (Figure 4, Vgh and Vgl). APA fails to teach of dividing the normal drive period into a data input period and a reset period; supplying a gate reset voltage sequentially to the gate lines to make an average voltage of 'liquid crystal cells higher than the transition voltage for the reset period; and supplying a data reset voltage to the data lines in accordance with the gate reset voltage. Kondoh discloses of dividing the normal drive period into a data input period and a reset period (Figure 11, RS is the reset period and the data input

period consists of Se and NSe, where RS, Se and NSe make a normal drive period); supplying a gate reset voltage sequentially to the gate lines to make an average voltage of 'liquid crystal cells higher than the transition voltage for the reset period (Paragraph [0009], lines 44-48); and supplying a data reset voltage to the data lines in accordance with the gate reset voltage (Figure 4, items (a), (b) and (c). Column 2, lines 27-34. The examiner interprets the scanning electrode to be the gate electrode connected to the gate lines and the signal electrode to be the data electrode connected to the data lines. Since the reset is occurring in graphs (a) and (b), there is a data reset voltage that is being applied to the data lines that happens in accordance with the reset applied to the gate lines). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teaching of APA and Kondoh in order to provide a liquid crystal display that can reset its gate lines and data lines before each transmission of data.

Regarding claim 11, APA and Kondoh disclose the liquid crystal display according to claim 10. APA also discloses wherein supplying the gate high and gate low voltages includes supplying the gate high voltage to the gate lines during anon-period for the thin film transistor, and supplying the gate low voltage to the gate lines during an off-period for the thin film transistor (Paragraph [0012] where it states: "Scan pulses (SP) with the gate high voltage Vgh turn on the TFT switch...", and to supply the gate low voltage to the gate lines during an off-period for the thin film transistor (Paragraph [0012] where it states: "As the gate high voltage Vgh supplied to the gate lines GL1 to GLn is changed to the gate low voltage Vgl, the TFT is turned off..."). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the

teaching of APA and Kondoh in order to only have the TFT on when data signals are being sent.

10. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over APA and Kondoh (EP 1,043,618 A1) and further in view Kwag (US 2002/0015017).

Regarding claim 12, APA and Kondoh disclose the liquid crystal display according to claim 10. APA and Kondoh fail to teach of a liquid crystal display wherein the gate reset voltage is a designated voltage set to be lower than the gate low voltage. Kwag discloses wherein the gate reset voltage is a designated voltage set to be lower than the gate low voltage (In Figure 7B, Vg(n-1), the voltage during the reset period is less than the voltage line during the overshoot interval, where the overshoot interval is when the gate low voltage is applied). Therefore it would have obvious to "one of ordinary skill" in the art to combine the teachings of APA, Kondoh and Kwag in order to reduce the average voltage of the liquid crystal display.

11. Claims 13-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over APA and Kondoh (EP 1,043,618 A1) and further in view of Ono et al. (US 6,057,817).

Regarding claim 13, APA and Kondoh disclose the liquid crystal display according to claim 10. APA and Kondoh fail to teach of a liquid crystal device wherein the gate reset voltage and the gate low voltage, which are alternated, constitute an AC voltage. Ono et al. disclose a liquid crystal device wherein the gate reset voltage and the gate low voltage, which are alternated, constitute an AC voltage (Figure 32, where

T_{S1} is the reset period in which $-V_R$ is the reset voltage and $+V_R$ is the gate low voltage, which are alternated applied during T_{S1}.). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings APA, Kondoh and Ono et al. in order to produce a liquid crystal display which has a reset period consisting of an AC voltage which allows for a decrease in power consumption by the liquid crystal while still providing for the average voltage applied to the liquid crystal to be higher than a transition voltage to prevent the display from changing into a splay state.

Regarding claim 14, APA, Kondoh and Ono et al. disclose the liquid crystal display according to claim 13. Kondoh also discloses wherein a half period of the AC voltage is set to be less than a response time of the liquid crystals (Column 9, lines 48-50. The examiner interprets that since the bipolar pulse, AC voltage, duration is 100μs that the half period is 50μs, which is much less than the response time of the liquid crystals since it is well known that liquid crystal response times are longer than 50μs). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings of APA, Kondoh and Ono et al. in order to prevent to the liquid crystals from responding and thus improving the brightness of the display.

Regarding claim 15, APA and Kondoh disclose the liquid crystal display according to claim 10. APA and Kondoh fail to teach of a liquid crystal device wherein the gate low voltage applied for the data input period is the same as an average value of the AC voltage. Ono et al. disclose a liquid crystal device wherein the gate low voltage applied for the data input period is the same as an average value of the AC voltage (Figure 32, The data input period is T_D, where in the gate low voltage shown in

the figure is the same as the average value of $-V_R$ and $+V_R$, which combine to form the AC voltage). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings of APA, Kondoh and Ono et al. in order to create a liquid crystal display that when the gate low voltage is applied during the data input period the average voltage applied to the liquid crystal is still higher than a transition voltage to prevent the display from changing into a splay state.

Regarding claim 16, APA, Kondoh and Ono et al. disclose the liquid crystal display according to claim 13. Kondoh also discloses wherein the gate high voltage is applied at least two times for the data input period (Figure 3 (a). The examiner interprets that the data input period to be a combination of Se and NSe, where the gate high voltage is applied twice during the selection period (Se) once with a negative polarity and once with a positive polarity and the gate low voltage was applied during the non selection period (NSe).). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings of APA, Kondoh and Ono et al. in order to compensate for the DC component which is created to cause the pixel voltage applied to the liquid crystal cell on the liquid crystal display panel to be biased to the negative polarity.

Regarding claim 17, APA and Kondoh disclose the liquid crystal display according to claim 10. APA and Kondoh fail to teach of a liquid crystal display wherein the gate reset voltage is an AC voltage having positive and negative polarities alternated on the basis of the gate low voltage for each frame. Ono et al. also discloses wherein the gate reset voltage is an AC voltage having positive and negative polarities

alternated on the basis of the gate low voltage for each frame (Figure 32, T_{S1} is the reset period and $+V_R$ is the positive polarity and $-V_R$ is the negative polarity. $+V_R$ and $-V_R$ are alternated based on the gate low voltage, which is 0 during the period T_S). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings APA, Kondoh and Ono et al. in order to produce a liquid crystal display which alternates between positive and negative polarities which allows for a decrease in power consumption by the liquid crystal while still providing for the average voltage applied to the liquid crystal to be higher than a transition voltage to prevent the display from changing into a splay state.

Regarding claim 18, APA and Kondoh disclose the liquid crystal display according to claim 10. APA and Kondoh fail to teach of a liquid crystal display wherein the gate reset voltage is an AC voltage. Ono et al. disclose a liquid crystal device wherein the gate reset voltage is an AC voltage (Figure 32, $+V_R$ and $-V_R$ constitute as an AC voltage). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings APA, Kondoh and Ono et al. in order to produce a liquid crystal display which has an AC reset voltage which allows for a decrease in power consumption by the liquid crystal while still providing for the average voltage applied to the liquid crystal to be higher than a transition voltage to prevent the display from changing into a splay state.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard can be reached on (571) 272-7603. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

24 August 2005

REGINA LIANG
PRIMARY EXAMINER